Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims:

1-38. (Canceled)

39. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a channel region formed in said semiconductor substrate;

a source region and a drain ~~regions~~ region in said semiconductor substrate wherein said channel region is located between said source region and said drain ~~regions~~ region;

at least first and second impurity regions formed in said channel region wherein said first impurity region is in contact with one of the source region and the drain ~~regions~~ region, said second impurity region is in contact with said one of the source region and the drain ~~regions~~ region, and said first and second impurity regions are doped with an impurity of a conductivity type opposite to said source region and said drain ~~regions~~ region;

a gate insulating film formed over the channel region; and

a gate electrode over the channel region with the gate insulating film interposed therebetween,

wherein said first and second impurity regions are separated from each other.

40. (Previously Presented) The semiconductor device according to claim 39 wherein said first and second impurity regions contain the impurity at a concentration within a range of 1×10^{17} to 5×10^{19} atoms/cm^3.

41. (Previously Presented) The semiconductor device according to claim 39 wherein a width of said first and second impurity regions along a channel width direction is 0.05 to 0.3 μm.

42. (Previously Presented) The semiconductor device according to claim 39 wherein an interval between said first and second impurity regions is 0.04 to 0.6 μm.

43. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate;

a channel region formed in said semiconductor substrate;

source and drain regions in said semiconductor substrate wherein said channel region is located between said source and drain regions;

at least first and second impurity regions formed in said channel region, wherein said first and second impurity regions are in contact with the source region and are separated from each other;

at least third and fourth impurity regions formed in said channel region, wherein said third and fourth impurity regions are in contact with the drain region and are separated from each other;

a gate insulating film formed over the channel region; and

a gate electrode over the channel region with the gate insulating film interposed therebetween,

wherein each of said first, second, third and fourth impurity regions is doped with an impurity of a conductivity type opposite to that of said source and drain regions.

44. (Previously Presented) The semiconductor device according to claim 43 wherein said first and second impurity regions contain an impurity at a concentration within a range of 1 x 10^{17} to 5 x 10^{19} atoms/cm^3.

45. (Previously Presented) The semiconductor device according to claim 43 wherein said third and fourth impurity regions contain an impurity at a concentration within a range of 1 x 10^{17} to 5 x 10^{19} atoms/cm^3.

46. (Previously Presented) The semiconductor device according to claim 43 wherein a width of said first and second impurity regions along a channel width direction is 0.05 to 0.3 μm.

47. (Previously Presented) The semiconductor device according to claim 43 wherein a width of said third and fourth impurity regions along a channel width direction is 0.05 to 0.3 μm.

48. (Previously Presented) The semiconductor device according to claim 43 wherein an interval between said first and second impurity regions is 0.04 to 0.6 μm.

49. (Previously Presented) The semiconductor device according to claim 43 wherein an interval between said third and fourth impurity regions is 0.04 to 0.6 μm.

50. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a channel region formed in said semiconductor substrate;

a source region and a drain ~~regions~~ region in said channel region wherein said channel region is located between said source region and said drain ~~regions~~ region;

at least first and second impurity regions formed in said channel region, wherein said first and second impurity regions are in contact with the same one of the source region and the drain ~~regions~~ region;

a gate insulating film formed over the channel region; and

a gate electrode over the channel region with the gate insulating film interposed therebetween,

wherein said first and second impurity regions are separated from each other and are doped with an impurity of a conductivity type opposite to said source region and said drain ~~regions~~ region, and

wherein said first and second impurity regions are overlapped by said gate electrode at least partly.

51. (Previously Presented) The semiconductor device according to claim 50 wherein said first and second impurity regions contain an impurity at a concentration within a range of 1 x 10^{17} to 5 x 10^{19} atoms/cm^3.

52. (Previously Presented) The semiconductor device according to claim 50 wherein a width of said first and second impurity regions along a channel width direction is 0.05 to 0.3 μm.

53. (Previously Presented) The semiconductor device according to claim 50 wherein an interval between said first and second impurity regions is 0.04 to 0.6 μm.

54. (Currently Amended) A semiconductor device comprising:

a semiconductor substrate;

a channel region formed in said semiconductor substrate;

a source region and a drain ~~regions~~ region in said semiconductor substrate wherein said channel region is located between said source region and said drain ~~regions~~ region wherein each of said source region and said drain ~~regions~~ region is provided with a metal silicide layer on a surface thereof;

at least first and second impurity regions formed in said channel region wherein said first and second impurity regions are in contact with the same one of the source region and the drain ~~regions~~ region and are separated from each other;

a gate insulating film formed over the channel region; and

a gate electrode over the channel region with the gate insulating film interposed therebetween,

wherein said first and second impurity regions are doped with an impurity of a conductivity type which is opposite to said region and said drain ~~regions~~ region.

55. (Previously Presented) The semiconductor device according to claim 54 wherein said metal silicide layer comprises titanium silicide.

56. (Previously Presented) The semiconductor device according to claim 54 wherein said first and second impurity regions contain the impurity at a concentration within a range of 1 x 10^{17} to 5 x 10^{19} atoms/cm^3.

57. (Previously Presented) The semiconductor device according to claim 54 wherein a width of said first and second impurity regions along a channel width direction is 0.05 to 0.3 μm.

58. (Previously Presented) The semiconductor device according to claim 54 wherein an interval between said first and second impurity regions is 0.04 to 0.6 μm.

59. (Previously Presented) The semiconductor device according to claim 39 further comprising at least third and fourth impurity regions formed in said channel region wherein said third and fourth impurity regions are in contact with the other one of the source and drain regions and said third and fourth impurity regions are separated from each other and are doped with an impurity of a conductivity type opposite to said source and drain regions.

60. (Previously Presented) The semiconductor device according to claim 50 further comprising at least third and fourth impurity regions formed in said channel region wherein said third and fourth impurity regions are in contact with the other one of the source and drain regions

and said third and fourth impurity regions are separated from each other and are doped with an impurity of a conductivity type opposite to said source and drain regions.

61. (Previously Presented) The semiconductor device according to claim 54 further comprising at least third and fourth impurity regions formed in said channel region wherein said third and fourth impurity regions are in contact with the other one of the source and drain regions and said third and fourth impurity regions are separated from each other and are doped with an impurity of a conductivity type opposite to said source and drain regions.

62-65. (Canceled)